Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARTIN KERBER

Appeal No. 1999-2576
Application 08/836,960[1]

ON BRIEF

Before MARTIN, BARRETT, and FLEMING, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3. Claim 4 has been canceled and claims 5 and 6 have been withdrawn as directed to a nonelected invention.

We reverse.

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[1] Application for patent filed May 22, 1997.

A. The invention

The invention is a lateral bipolar transistor having the following construction:

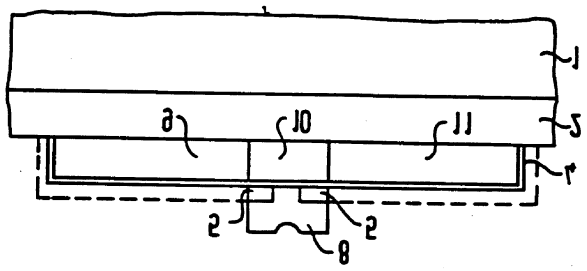


FIG 5

Numeral 1 designates a bulk layer of SOI (silicon-on-insulator) substrate. Layer 2 is an insulator layer. Numerals 9-11 respectively designate the emitter, base, and collector regions of a silicon layer, upon which has been formed a silicon nitride diffusion barrier layer 4. After a silicon oxide layer 5 has been formed on nitride layer 4 and a polysilicon base electrode 8 is formed in and around an opening in layer 5, the portions of layer 5 outside the base electrode are removed, as indicated by the dashed lines. In the resulting device, polysilicon base electrode 8 is

separated from base region 10 by nitride diffusion barrier layer 4, which

> prevents further diffusion of the dopant from the polysilicon of the base electrode into the silicon of the base region 10. However, the diffusion barrier is thin enough to enable the charge carriers to pass virtually unhindered from the base electrode 8 into the base region 10 (tunnel effect), thereby giving a small base supply resistance.

Specification at 4, ll. 8-12.

B. The claims

Claim 1, the sole independent claim, reads as follows:

> 1. A lateral bipolar transistor comprising: an emitter region, a base region and a collector region in a semiconductor layer; a base terminal region; on said base region, a base electrode which is made up of doped polysilicon material and which is separated from said base region by a nitride diffusion barrier; said diffusion region having a thickness that is thin enough to enable charge carriers to pass through said diffusion barrier such that the transistor functions; said base electrode being electrically conductively connected to said base terminal region.

Appellant treats claims 2 and 3 as standing or falling with claim 1. Brief at 4.

C. The references and rejection

The examiner relies on the following references:

McFarlane et al. (McFarlane) 5,355,015 (US) Oct. 11, 1994

Yorikane[2] 61-242072 (JP) Oct. 28, 1996

Edholm et al. (Edholm), A self-Aligned Lateral Bipolar Transistor Realized on SIMOX-Material, 40 IEEE Transactions on Electron Devices 2359-2360 (Dec. 1993).

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as unpatentable for obviousness over Edholm in view of McFarlane and Yorikane.

The examiner describes Edholm Figure 1, reproduced below, as disclosing "an SOI [silicon-on-insulator] transistor structure but fail[ing] to explicitly disclose the use of a silicon nitride barrier layer formed between the polysilicon base electrode and the underlying base region" (Answer at 3):

[2] Our understanding of this reference is based on a translation obtained by the PTO (copy attached), which gives the inventor's name as Yorigane instead of Yorikane, the name appearing in the English-language abstract.

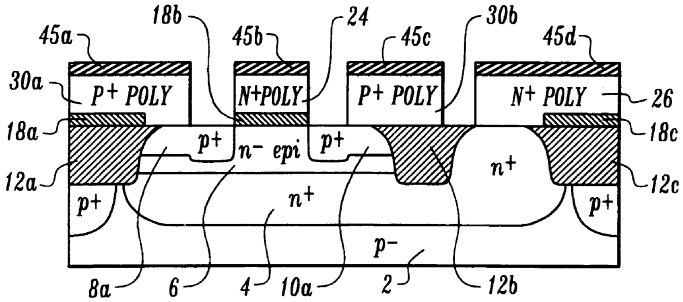
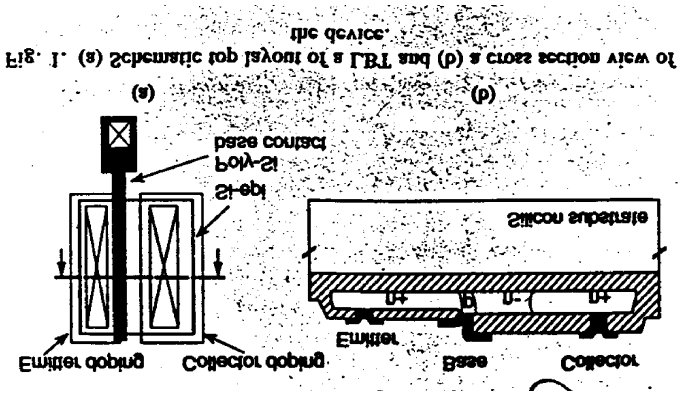


FIG. 11.

To remedy this deficiency in Edholm, the examiner relies on McFarlane and Yorikane. McFarlane discloses a lateral transistor (see title) of the bipolar type (see col. 4, l. 51) having the following structure:



P regions 8a and 10a constitute the collector and emitter respectively, while N- epitaxial layer 6 constitutes the base. N+ poly region 24 is separated from base 6 by a silicon oxide layer 18b, which "prevents diffusion of the of the arsenic dopant into N- epi region 6 from N+ poly region 24" so that "[t]he base region of the transistor thus remains N- epi" (col. 4, ll. 53-56), thereby yielding "a transistor with breakdown voltages greater than conventional transistors fabricated such that the N+ poly is in contact with the N- epi base" (id. at ll. 56-59).

Also, the base contact includes a refractory metal interconnect 45b supported by a doped polysilicon contact layer 24, which is separated from the base region 6 by a diffusion barrier layer 18b of silicon oxide, formed as part of a grown oxide layer 14 (Fig. 2) (col. 3, ll. 41-52).

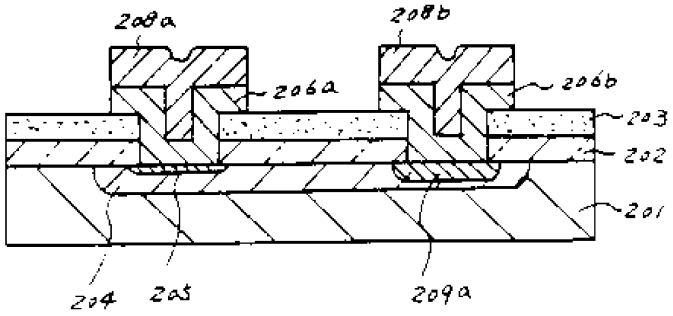
While P+ POLY regions 30a and 30b function as the collector and emitter contacts respectively (col. 4, ll. 47-49), appellant correctly notes (Brief at 6) that N+ POLY 24

region does not function as the "base contact." Instead, that function is performed by N+ POLY region 26 (col. 4, l. 50), which is coupled to base 6 through the N+ buried layer 4. Moreover, McFarlane gives this as the reason the alternative embodiment shown in Figure 12 omits the refractory layer 45b over N+ POLY layer 24 (col. 4, ll. 60-65). Nevertheless, Appellant's observation that

N+ POLY region does not function as the base terminal does not undercut the rejection, because claim 1 does not specify that the "diffusion barrier" separates the "base region" from the "base terminal region." Instead, the claim specifies that the "diffusion barrier" separates the "base region" from a "base electrode," which is satisfied when the term "base electrode" is read on N+ POLY region 24.

The examiner relies on Yorikane as broadly teaching "the use of [a] silicon nitride layer for the purpose of preventing diffusion of impurities between impurity doped regions." Answer at 3. Yorikane's Figure 6 reproduced below, shows a prior art transistor structure including an N-type substrate 201, a P-type base layer 204, an N-type emitter region 209, a

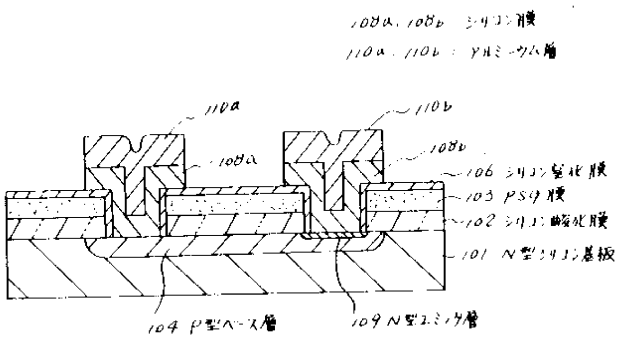
silicon oxide layer 202, a phospho-silicate glass (PSG) layer 203, and



第 6 図

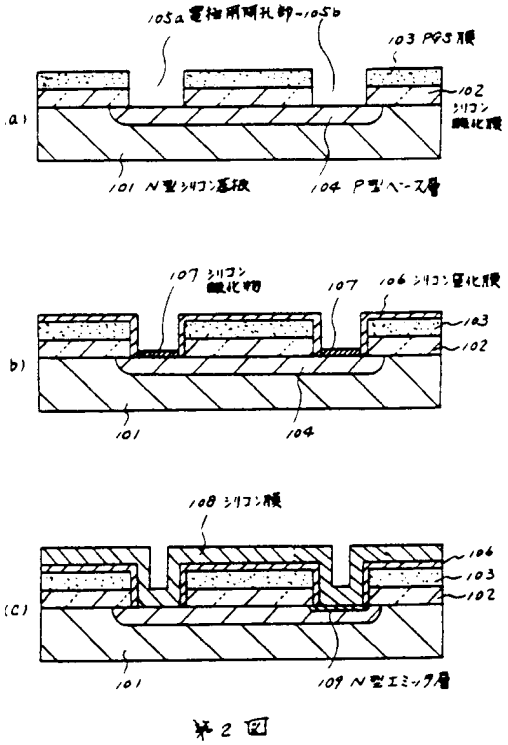
"silicone" (polysilicon) films 206a and 206b respectively supporting aluminum base and emitter electrodes 208a and 208b: In this structure phosphorus from PSG layer 203 diffuses into polysilicon contacts 206a and 206b and thereby into the base layer 204, creating an unwanted N-type layer 205 in the P-type base layer and causing N-type emitter 209a to be deeper than desired. Transl. at 4, 1st full para. Yorikane's solution, shown in Figure 1, is to form a silicone nitride layer 106 for

preventing direct contact between the PSG film 103 and the polysilicon layers 108a and 108b:



第1図

Figures 2(a)-(c) show the steps involved in forming this silicon nitride layer.:



第2図

As shown in Figure 2(a), after the silicon dioxide and PSG layers 102 and 103 have been formed on the substrate 101, holes 105a and 105b are formed therein. Referring to Figure 2(b), next a silicon nitride layer 106 is formed on the top of PSG layer 103, on the side walls of the holes, and

on the exposed parts of the base layer at the bottom of the holes, after which the silicon nitride layer at the bottom of the holes is converted to silicon oxide and removed using a fluoride type solution. Transl. at 6-7. The next step, shown in Figure 2(c), is to deposit the polysilicon film 108 of which polysilicon layers 108a and 108b will be formed.

Inasmuch as Yorikane fails to disclose forming a silicon nitride diffusion barrier layer between the base layer and its associated polysilicon layer, as required by claim 1, the question is whether it would have been obvious in view of Yorikane to replace McFarlane's diffusion barrier layer 18b with a layer of silicon nitride. However, even assuming for the sake of argument that such a substitution would have been obvious, we agree with Appellant that the references collectively fail to suggest making the silicon nitride layer thin enough to allow charge carriers to pass therethrough. Nor is this an inherent result of combining the teachings of McFarlane and Yorikane in the foregoing manner. Whereas Appellant's silicon nitride layer is "typically about 2 nm" (Specification at 3, l. 6), which is equivalent to about 20 D,

Yorikane's silicon nitride layer 106 is much thicker, at 500

D. Trans. at 7.

The § 103 rejection of claims 1-3 is therefore reversed.[3]

REVERSED

JOHN C. MARTIN Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)

JCM/sld

[3] We do not reach the question of whether claim 1 requires that the transistor be operated such that the charge carriers pass through the silicon nitride diffusion barrier or the question of whether it would have been obvious to use McFarlane's N+ POLY region 24 as the base terminal.

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Enclosure: Copy of translation of Yorikane.